



Subclass	Class	ISSUE CLASSIFICATION



PATENT NUMBER

## U.S. UTILITY Patent Application

O.I.P.E.	PATENT DATE
12W SCANNED 832 Q.A. CH	

APPLICATION NO. 09/707585	CONT/PRIOR	CLASS 713	SUBCLASS 330	ART UNIT 2182 2181	EXAMINER Butler AWE
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APPLICANTS  
TITLE

Gary Verdun

2185

Processor power state transistions using separate logic control

PTO-2040  
12/99

## ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)					
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
INTERNATIONAL CLASSIFICATION							

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<input type="checkbox"/> <b>TERMINAL DISCLAIMER</b>	<b>DRAWINGS</b>			<b>CLAIMS ALLOWED</b>	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	(Assistant Examiner) _____ (Date) _____			<b>NOTICE OF ALLOWANCE MAILED</b>	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____	(Primary Examiner) _____ (Date) _____			<b>ISSUE FEE</b>	
				Amount Due	Date Paid
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	(Legal Instruments Examiner) _____ (Date) _____			<b>ISSUE BATCH NUMBER</b>	

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